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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of : DANIELLE A. THOMAS
U.S. Serial No. : to be assigned
Filing Date : to be assigned
Prior U.S. Serial No. : 09/360,839
Prior Filing Date : July 26, 1999
Prior Examiner : N. Ha
Title : SCRATCH PROTECTION FOR DIRECT
CONTACT SENSORS

BOX PATENT APPLICATION

Commissioner of Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

Prior to the grant of the patent for United States Serial No. 09/360,839, the Applicant is filing a continuation application under 37 C.F.R. § 1.53(b). Before examination, please amend the application as follows:

IN THE SPECIFICATION:

Please replace the paragraph on page 2, lines 3–7 of the specification with the following:

The present invention is a continuation of commonly assigned copending

United States Serial No. 09/360,839, and is related to the subject matter of, and claims priority to, commonly assigned, copending United States Serial No. 09,364,307 entitled "SCRATCH RESISTANCE IMPROVEMENT BY FILLING METAL GAPS" and filed July 30, 1999. The content of the above-referenced related application is incorporated herein by reference.

Please replace the heading on page 6, line 1 of the specification with the following:

DESCRIPTION OF THE INVENTION

Please replace the paragraph on page 7, line 24 through page 8, line 3 of the specification with the following:

Figure 1C is a cross-sectional detail of a sensor array cell as seen from a cross-section taken along section line A-A. Sensor circuit **102** within a sensor array cell includes one or more active areas, such as polysilicon electrodes **102** or source/drain regions **122** within a substrate **124**. A dielectric **126** overlies active areas **120**, **122**, with openings through which metal contacts **128** are formed to connect active regions **120**, **122** with metal regions **130** (e.g., landing pads or interconnects) within the first metallization level. An intermetal dielectric **132**

overlies metal regions 130 and dielectric 126, with openings therethrough in which are formed metal vias 134 connecting metal regions 130 to capacitive electrodes 136 overlying the interlevel dielectric 132.

Please replace the paragraph on page 8, lines 5–9 of the specification with the following:

Capacitive electrodes 136 are covered by a second intermetal dielectric 138, on which are formed electrostatic discharge (ESD) protection patterns 140. A passivation layer 142, which may actually comprise multiple layers, covers the ESD protection lines 140 and forms the surface 144 which is contacted by the epidermal layer of the finger during fingerprint acquisition.

IN THE CLAIMS:

Please cancel claims 10–13 without prejudice. Please amend the remaining claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (amended) An integrated circuit structure, comprising:

a capacitive electrode proximate to a sensing surface on which an object is selectively placed,
the capacitive electrode forming a capacitor with the object when the object is placed on the sensing
surface;

a dielectric underlying the capacitive electrode; and

an active region underlying the dielectric,

wherein the capacitive electrode and all conductive regions between the capacitive electrode
and the active region are formed of a conductive material having a hardness greater than a hardness
of aluminum.

2. (unchanged) The integrated circuit structure of claim 1, wherein the capacitive electrode and each
conductive region between the capacitive electrode and the active region are formed of a conductive
material having a hardness at least as great as a hardness of the dielectric.

1 3. (amended) The integrated circuit structure of claim 1, further comprising:

2 a passivation layer over the capacitive electrode, the passivation layer forming the sensing
3 surface,

4 wherein the capacitive electrode and all conductive regions between the capacitive electrode
5 and the active region are formed of a conductive material having a hardness at least as great as a
6 hardness of the passivation layer.

1 4. (amended) The integrated circuit structure of claim 1, wherein the capacitive electrode and all
2 conductive regions between the capacitive electrode and the active region are formed of tungsten.

1 5. (unchanged) The integrated circuit structure of claim 4, further comprising:

2 a tungsten via beneath the capacitive electrode.

1 6. (unchanged) The integrated circuit structure of claim 5, further comprising:

2 a tungsten interconnect beneath the via.

1 7. (unchanged) The integrated circuit structure of claim 6, further comprising:

2 a tungsten contact between the interconnect and the active region.

8. (unchanged) The integrated circuit structure of claim 7, wherein the active region is a gate electrode.

9. (amended) An integrated circuit structure, comprising:

an active region;

a dielectric overlying the active region and having a contact opening therethrough;

a tungsten contact within the contact opening;

a tungsten metal region overlying the contact and a portion of the dielectric;

an interlevel dielectric overlying the tungsten metal region and the dielectric and having an opening therethrough;

a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel dielectric, wherein the capacitive electrode is proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is placed on the sensing surface and is electrically connected to the active region by the contact, the metal region, and the via.

1 14. (amended) A method of forming a scratch resistant integrated circuit structure, comprising:
2 forming an active region;
3 forming a dielectric overlying the active region; and
4 forming a capacitive electrode overlying the dielectric proximate to a sensing surface on
5 which an object is selectively placed, the capacitive electrode forming a capacitor with the object
6 when the object is placed on the sensing surface, wherein the capacitive electrode and each
7 conductive region between the capacitive electrode and the active region are formed of a conductive
8 material having a hardness greater than a hardness of aluminum.

1 15. (unchanged) The method of claim 14, wherein the capacitive electrode and each conductive
2 region between the capacitive electrode and the active region are formed of a conductive material
3 having a hardness at least as great as a hardness of the dielectric.

1 16. (amended) The method of claim 14, further comprising:

2 forming a passivation layer over the capacitive electrode, the passivation layer forming the
3 sensing surface,

4 wherein the capacitive electrode and all conductive regions between the capacitive electrode
5 and the active region are formed of a conductive material having a hardness at least as great as a
6 hardness of the passivation layer.

1 17. (amended) The method of claim 14, wherein the capacitive electrode and all conductive regions
2 between the capacitive electrode and the active region are formed of tungsten.

1 18. (unchanged) The method of claim 17, further comprising:
2 forming a tungsten via beneath the capacitive electrode.

1 19. (unchanged) The method of claim 18, further comprising:
2 forming a tungsten interconnect beneath the via.

1 20. (unchanged) The method of claim 19, further comprising:
2 forming a tungsten contact between the interconnect and the active region.

1 21. (unchanged) The method of claim 20, wherein the active region is a gate electrode.

1 22. (amended) A method of forming an integrated circuit structure, comprising:

2 forming an active region;

3 forming a dielectric overlying the active region and having a contact opening therethrough;

4 forming a tungsten contact within the contact opening;

5 forming a tungsten metal region overlying the contact and a portion of the dielectric;

6 forming an interlevel dielectric overlying the tungsten metal region and the dielectric and
7 having an opening therethrough;

8 forming a tungsten via within the opening through the interlevel dielectric; and

9 forming a tungsten capacitive electrode overlying the tungsten via and a portion of the
10 interlevel dielectric, wherein the capacitive electrode is proximate to a sensing surface on which an
11 object is selectively placed, the capacitive electrode forming a capacitor with the object when the
12 object is placed on the sensing surface and is electrically connected to the active region by the
13 contact, the metal region, and the via.

1 23. (unchanged) The method of claim 22, further comprising:

2 forming an oxide over the capacitive electrode and the interlevel dielectric adjacent the
3 capacitive electrode;

4 forming a passivation layer including a silicon nitride layer and a silicon carbide layer over
5 the oxide; and

6 forming tungsten ESD protection within the passivation layer.

1 24. (amended) A method of forming a scratch resistant integrated circuit structure, comprising:

2 forming a plurality of active regions;

3 forming a dielectric over the plurality active regions; and

4 forming an array of capacitive electrodes overlying the dielectric proximate to a sensing
5 surface on which an object is selectively placed, the capacitive electrodes each forming a capacitor
6 with the object when the object is placed on the sensing surface and wherein the capacitive
7 electrodes are each formed of a conductive material having a hardness at least as great as a hardness
8 of the dielectric.

1 25. (amended) The method of claim 24, wherein the step of forming an array of capacitive
2 electrodes overlying the dielectric of a conductive material having a hardness at least as great as a
3 hardness of the dielectric further comprises:

4 forming the array of capacitive electrodes of a conductive material having a hardness at least
5 as great as a hardness of a passivation layer overlying the array of conductive electrodes and forming
6 the sensing surface.

1 26. (unchanged) The method of claim 24, wherein the step of forming an array of capacitive
2 electrodes overlying the dielectric of a conductive material having a hardness at least as great as a
3 hardness of the dielectric further comprises:

4 forming the array of capacitive electrodes of tungsten.

1 27. (unchanged) The method of claim 24, further comprising:

2 forming each metallization region between the array of capacitive electrodes and the plurality
3 of active regions of a conductive material having a hardness at least as great as the hardness of the
4 dielectric.

REMARKS:

Claims 1–9 and 14–27 are pending in the present application.

Claims 1, 3–4, 9, 14, 16–17, 22 and 24–25 were amended to clarify features of the invention without altering the claim scope.

The specification was amended to correct errors therein. No new matter has been added to the specification.

Examination of the application on the merits is respectfully requested.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

The paragraph on page 2, lines 3–7 of the specification was amended herein as follows:

The present invention is a continuation of commonly assigned copending United States Serial No. 09/360,839, and is related to the subject matter of, and claims priority to, commonly assigned, copending United States [patent applications serial no. [09/____,____ (Docket No. 99-C-087)]Serial No. 09,364,307 entitled “SCRATCH RESISTANCE IMPROVEMENT BY FILLING METAL GAPS” and filed [_____] July 30, 1999. The content of the above-referenced related application is incorporated herein by reference.

The heading on page 6, line 1 of the specification was amended herein as follows:

DESCRIPTION OF THE [PREFERRED EMBODIMENT]INVENTION

The paragraph on page 7, line 24 through page 8, line 3 of the specification was amended herein as follows:

Figure 1C is a cross-sectional detail of a sensor array cell as seen from a cross-section taken along section line A-A. Sensor circuit **102** within a sensor array

cell includes one or more active areas, such as polysilicon electrodes **102** or source/drain regions **122** within a substrate **124**. A dielectric **126** overlies active areas **120**, **122**, with openings through which metal contacts **128** are formed to connect active regions **120**, **122** with metal regions **130** (e.g., landing pads or interconnects) within the first metallization level. An intermetal dielectric **132** overlies metal regions **130** and dielectric **126**, with openings therethrough in which are formed metal vias **134** connecting metal regions **130** to capacitive electrodes **136** overlying the interlevel dielectric **[134]132**.

The paragraph on page 8, lines 5–9 of the specification was amended herein as follows:

Capacitive electrodes **136** are covered by a second intermetal dielectric **138**, on which are formed electrostatic discharge (ESD) protection patterns **140**. A passivation layer **142**, which may actually comprise multiple layers, covers the ESD protection lines **[142]140** and forms the surface **144** which is contacted by the epidermal layer of the finger during fingerprint acquisition.

Claims 1, 3–4, 9, 14, 16–17, 22 and 24–25 were amended herein as follows:

1. (amended) An integrated circuit structure, comprising:

a capacitive electrode proximate to a sensing surface on which an object is selectively placed,
the capacitive electrode forming a capacitor with the object when the object is placed on the sensing
surface;

a dielectric underlying the capacitive electrode; and

an active region underlying the dielectric,

wherein the capacitive electrode and [each]all conductive [region]regions between the
capacitive electrode and the active region are formed of a conductive material having a hardness
greater than a hardness of aluminum.

3. (amended) The integrated circuit structure of claim 1, further comprising:

a passivation layer over the capacitive electrode, the passivation layer forming the sensing
surface,

wherein the capacitive electrode and [each]all conductive [region]regions between the
capacitive electrode and the active region are formed of a conductive material having a hardness at
least as great as a hardness of the passivation layer.

1 4. (amended) The integrated circuit structure of claim 1, wherein the capacitive electrode and
2 [any]all conductive regions between the capacitive electrode and the active region are formed of
3 [tunsten]tungsten.

1 9. (amended) An integrated circuit structure, comprising:

2 an active region;

3 a dielectric overlying the active region and having a contact opening therethrough;

4 a tungsten contact within the contact opening;

5 a tungsten metal region overlying the contact and a portion of the dielectric;

6 an interlevel dielectric overlying the tungsten metal region and the dielectric and having an
7 opening therethrough;

8 a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel
9 dielectric, wherein the capacitive electrode is proximate to a sensing surface on which an object is
10 selectively placed, the capacitive electrode forming a capacitor with the object when the object is
11 placed on the sensing surface and is electrically connected to the active region by the contact, the
12 metal region, and the via.

1 14. (amended) A method of forming a scratch resistant integrated circuit structure, comprising:
2 forming an active region;
3 forming a dielectric overlying the active region; and
4 forming a capacitive electrode overlying the dielectric proximate to a sensing surface on
5 which an object is selectively placed, the capacitive electrode forming a capacitor with the object
6 when the object is placed on the sensing surface, wherein the capacitive electrode and each
7 conductive region between the capacitive electrode and the active region are formed of a conductive
8 material having a hardness greater than a hardness of aluminum.

1 16. (amended) The method of claim 14, further comprising:
2 forming a passivation layer over the capacitive electrode, the passivation layer forming the
3 sensing surface,
4 wherein the capacitive electrode and [each]all conductive [region]regions between the
5 capacitive electrode and the active region are formed of a conductive material having a hardness at
6 least as great as a hardness of the passivation layer.

1 17. (amended) The method of claim 14, wherein the capacitive electrode and [each]all conductive
2 [region]regions between the capacitive electrode and the active region are formed of tungsten.

22. (amended) A method of forming an integrated circuit structure, comprising:

forming an active region;

forming a dielectric overlying the active region and having a contact opening therethrough;

forming a tungsten contact within the contact opening;

forming a tungsten metal region overlying the contact and a portion of the dielectric;

forming an interlevel dielectric overlying the tungsten metal region and the dielectric and having an opening therethrough;

forming a tungsten via within the opening through the interlevel dielectric; and

forming a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel dielectric, wherein the capacitive electrode is proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is placed on the sensing surface and is electrically connected to the active region by the contact, the metal region, and the via.

1 24. (amended) A method of forming a scratch resistant integrated circuit structure, comprising:
2 forming a plurality of active regions;
3 forming a dielectric over the plurality active regions; and
4 forming an array of capacitive electrodes overlying the dielectric proximate to a sensing
5 surface on which an object is selectively placed, the capacitive electrodes each forming a capacitor
6 with the object when the object is placed on the sensing surface and wherein the capacitive
7 electrodes are each formed of a conductive material having a hardness at least as great as a hardness
8 of the dielectric.

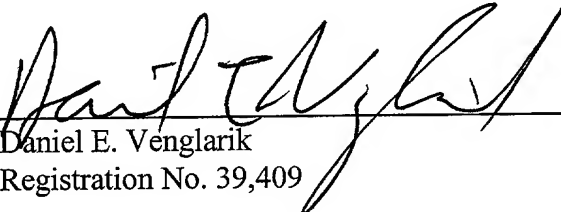
1 25. (amended) The method of claim 24, wherein the step of forming an array of capacitive
2 electrodes overlying the dielectric of a conductive material having a hardness at least as great as a
3 hardness of the dielectric further comprises:
4 forming the array of capacitive electrodes of a conductive material having a hardness at least
5 as great as a hardness of a passivation layer overlying the array of conductive electrodes and forming
6 the sensing surface.

The Applicant believes that this Applications in condition for allowance. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting prosecution of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@novakov.com*.

Respectfully submitted,

NOVAKOV DAVIS & MUNCK, P.C.

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